CLAIMS

What is claimed is:

1. A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch routing paths of packets received through mediums coupled to the ingress/egress points;

a first buffering structure including a first plurality of storage structures and first associated packet diversion and insertion logic, coupled to a first of said ingress/egress point to facilitate at least a selected one of diversion of selected ones of a first plurality of egress packets being routed through said first ingress/egress point onto a first one of said mediums, and insertion of additional ones into said first plurality of egress packets being routed; and

a second buffering structure including a second plurality of storage structures and second associated packet diversion and insertion logic, coupled to a second of said ingress/egress points to facilitate at least a selected one of diversion of selected ones of a second plurality of egress packets being routed through said second ingress/egress point onto a second one of said mediums, and insertion of additional ones into said second plurality of egress packets being routed.

2. The apparatus of claim 1, wherein said first buffering structure comprises

a first storage structure to stage undiverted ones of said egress packets;

a second storage structure to stage diverted ones of said egress packets;

a divert logic coupled to the first ingress/egress point and said first and second storage structures to selective route said egress packets from said first

ingress/egress point onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said egress packets in unpacked portions.

3. The apparatus of claim 1, wherein said first buffering structure comprises

a first storage structure coupled to the first ingress/egress point to stage undiverted ones of said egress packets;

a second storage structure to stage insertion ones of said egress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said egress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said egress packets.

4. The apparatus of claim 1, wherein said first buffering structure further facilitates at least an additional selected one of diversion of selected ones of a first plurality of ingress packets being received from said first medium into said switching fabric through said first ingress/egress point, and insertion of additional ones into said first plurality of ingress packets being received.

5. The apparatus of claim 4, wherein said first buffering structure comprises

a first storage structure to stage undiverted ones of said ingress packets;

a second storage structure to stage diverted ones of said ingress packets;

a divert logic coupled to the first medium and said first and second storage structures to selective route said ingress packets received from said first medium onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said ingress packets in unpacked portions.

6. The apparatus of claim 4, wherein said first buffering structure comprises

a first storage structure coupled to the first medium to stage undiverted ones of said ingress packets;

a second storage structure to stage insertion ones of said ingress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said ingress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said ingress packets.

7. The apparatus of claim 4, wherein said second buffering structure further facilitates at least an additional selected one of diversion of selected ones of a second plurality of ingress packets being received from said second medium into said switching fabric through said second ingress/egress point, and insertion of additional ones into said second plurality of ingress packets being received.

8. A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch routing paths of packets received through mediums coupled to the ingress/egress points;

a first buffering structure including a first plurality of storage structures and first associated packet diversion and insertion logic, coupled to a first of said ingress/egress points to facilitate at least a selected one of diversion of selected ones of a first plurality of ingress packets being received from a first one of said mediums into said switching fabric through said first ingress/egress point, and insertion of additional ones into said first plurality of ingress packets being received; and

a second buffering structure including a second plurality of storage structures and second associated packet diversion and insertion logic, coupled to a second of said ingress/egress points to facilitate at least a selected one of diversion of selected ones of a second plurality of ingress packets being received from a second one of said mediums into said switching fabric through said second ingress/egress point, and insertion of additional ones into said second plurality of ingress packets being received.

9. The apparatus of claim 8, wherein said first buffering structure comprises

a first storage structure to stage undiverted ones of said ingress packets;

a second storage structure to stage diverted ones of said ingress packets;

a divert logic coupled to the first medium and said first and second storage structures to selective route said ingress packets received from said first medium onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said ingress packets in unpacked portions.

10. The apparatus of claim 8, wherein said first buffering structure comprises

a first storage structure coupled to the first medium to stage undiverted ones of said ingress packets;

a second storage structure to stage insertion ones of said ingress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said ingress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said ingress packets.

11. A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch packets received through mediums coupled to the ingress/egress points; and

a buffering structure including

a first plurality of storage structures and first associated packet diversion and insertion logic, coupled to a first of said ingress/egress points, to facilitate at least a selected one of diversion of selected ones of a plurality of ingress packets being received from a first one of said mediums into said switching fabric through said first ingress/egress point, and insertion of additional ones into said plurality of ingress packets being received, and

a second buffering structure including a second plurality of storage structures and second associated packet diversion and insertion logic, coupled to the first ingress/egress point, to facilitate at least a selected one of diversion of selected ones of a plurality of egress packets being routed through said first ingress/egress point onto said first medium, and insertion of additional ones into said plurality of ingress packets being routed.

12. The apparatus of claim 11, wherein said first plurality of storage structures and associated first packet diversion and insertion logic comprises

a first storage structure to stage undiverted ones of said egress packets;

a second storage structure to stage diverted ones of said egress packets;

a divert logic coupled to the first ingress/egress point and said first and second storage structures to selective route said egress packets from said first ingress/egress point onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said egress packets in unpacked portions.

13. The apparatus of claim 11, wherein said first plurality of storage structures and associated first packet diversion and insertion logic comprises

a first storage structure coupled to the first ingress/egress point to stage undiverted ones of said egress packets;

a second storage structure to stage insertion ones of said egress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said egress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said egress packets.

14. The apparatus of claim 11, wherein said second plurality of storage structures and associated second packet diversion and insertion logic comprises

a first storage structure to stage undiverted ones of said ingress packets;

a second storage structure to stage diverted ones of said ingress packets;

a divert logic coupled to the first medium and said first and second storage structures to selective route said ingress packets received from said first medium onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said ingress packets in unpacked portions.

15. The apparatus of claim 11, wherein said second plurality of storage structures and associated second packet diversion and insertion logic comprises

a first storage structure coupled to the first medium to stage undiverted ones of said ingress packets;

a second storage structure to stage insertion ones of said ingress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said ingress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said ingress packets.

16. An optical networking module comprising:

an optical component to send and receive optical signals encoded with data transmitted through a coupled optical medium;

an optical-electrical component coupled to the optical component to encode digital data onto optical signals and to decode encoded digital data on optical signals back into their digital forms;

a data link/physical layer processing unit, including a buffering structure comprising a plurality of storage structures and associated packet diversion and insertion logic, coupled to the optical-electrical component and to a packet source/sink, to facilitate at least a selected one of data link/physical processing of ingress packets received from said optical medium for said packet source/sink and egress packets to be routed from said packet source/sink onto said optical medium, with each of said data link/physical processing of ingress and egress packets including at least a selected one of diversion of selected ones of a plurality of ingress/egress packets being received from/routed onto said optical medium, and insertion of additional ones into said plurality of ingress/egress packets being received/routed; and

a body encasing said optical component, said optical-electrical component, and said data link/physical processing unit as a single module.

17. The optical networking module of claim 16, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises

a first storage structure to stage undiverted ones of said egress packets;

a second storage structure to stage diverted ones of said egress packets;

a divert logic coupled to said packet source/sink and said first and second storage structures to selectively route said egress packets from said packet source/sink onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said egress packets in unpacked portions.

18. The optical networking module of claim 16, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises

a first storage structure coupled to the packet source/sink to stage undiverted ones of said egress packets;

a second storage structure to stage insertion ones of said egress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said egress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said egress packets.

19. The optical networking module of claim 16, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises

a first storage structure to stage undiverted ones of said ingress packets;

a second storage structure to stage diverted ones of said ingress packets;

a divert logic coupled to the optical medium and said first and second storage structures to selective route said ingress packets received from said optical medium onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said ingress packets in unpacked portions.

20. The optical networking module of claim 16, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises

a first storage structure coupled to the optical medium to stage undiverted ones of said ingress packets;

a second storage structure to stage insertion ones of said ingress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said ingress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said ingress packets.

21. The optical network module of claim 16, wherein said optical and optical-electrical components, said data link/physical layer processing unit are all designed to support data rates of at least 10GB/s.

22. The optical network module of claim 16, wherein said data link/physical layer processing unit is a multi-protocol processor that supports a plurality of datacom and telecom protocols.

23. A multi-protocol processor comprising:

a plurality of I/O interfaces to facilitate selective optical-electrical trafficking of data transmitted in accordance with a selected one of a plurality of datacom and telecom protocols;

a plurality of data link and physical sub-layer processing units selectively coupled to each other and to the I/O interfaces to be selectively employed in combination to perform selected data link and physical sub-layer processing on egress as well as ingress ones of said data, in accordance with said selected one of said plurality of protocols; and

a buffering structure coupled to at least a system-side one of said I/O interfaces and a media processing one of said data link and physical sub-layer processing units, including a plurality of storage structures and associated packet diversion and insertion logic to facilitate at least a selected one of diversion of selected ones of a plurality of egress packets, and insertion of additional ones into said plurality of egress packets, diversion of selected ones of a plurality of ingress packets, and insertion of additional ones into said plurality of ingress packets. .

24. The processor of claim 23, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises

a first storage structure to stage undiverted ones of said egress packets;

a second storage structure to stage diverted ones of said egress packets;

a divert logic coupled to said packet source/sink and said first and second storage structures to selectively route said egress packets from said packet source/sink onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said egress packets in unpacked portions.

25. The processor of claim 23, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises

a first storage structure coupled to the packet source/sink to stage undiverted ones of said egress packets;

a second storage structure to stage insertion ones of said egress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said egress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said egress packets.

26. The processor of claim 23, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises

a first storage structure to stage undiverted ones of said ingress packets;

a second storage structure to stage diverted ones of said ingress packets;

a divert logic coupled to the optical medium and said first and second storage structures to selective route said ingress packets received from said optical medium onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said ingress packets in unpacked portions.

27. The processor of claim 23, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises

a first storage structure coupled to the optical medium to stage undiverted ones of said ingress packets;

a second storage structure to stage insertion ones of said ingress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said ingress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said ingress packets.

28. The processor of claim 23, wherein said interfaces, said plurality of data link and physical sub-layer processing units and said buffering structure are all designed to support data rates of at least 10GB/s.

29. The processor of claim 23, wherein said processor is disposed on a single integrated circuit.

30. A buffering structure comprising:

a first storage structure to stage undiverted ones of egress packets;

a second storage structure to stage diverted ones of egress packets;

a third storage structure to stage insertion ones of egress packets;

a first divert logic coupled to said first and second storage structures to selectively route egress packets onto a selected one of said first and second storage structures;

a first insert logic coupled to said first and third storage structures to selectively merge said undiverted ones and said insertion ones of said egress packets; and

a register interface, including packet packing and unpacking logic, coupled to the second and third storage structures to facilitate retrieval by a processor said diverted ones of said egress packets in unpacked portions, and provision by said processor said insertion ones of said egress packets in unpacked portions.

31. The buffering structure of claim 30, wherein said buffering structure further comprises

a fourth storage structure to stage undiverted ones of ingress packets;

a fifth storage structure to stage diverted ones of ingress packets;

a second divert logic coupled to said fourth and fifth storage structures to selective route ingress packets onto a selected one of said fourth and fifth storage structures; and

said register interface, also coupled to the fifth storage structure to facilitate retrieval by said processor said diverted ones of said ingress packets in unpacked portions.

32. The buffering structure of claim 30, wherein

said buffering structure further comprises

a fourth storage structure to stage undiverted ones of ingress packets,

a fifth storage structure to stage insertion ones of ingress packets, and

an insertion logic coupled to the fourth and fifth storage structures to

selective merge said undiverted ones and said insertion ones of said ingress packets; and

said register interface is further coupled to said firth storage structures to facilitate provision to said fifth storage structure by said processor said insertion ones of said ingress packets in unpacked portions.

33. A buffering structure comprising:

a first storage structure to stage undiverted ones of ingress packets;

a second storage structure to stage diverted ones of ingress packets;

a third storage structure to stage insertion ones of ingress packets;

a first divert logic coupled to said first and second storage structures to selectively route ingress packets onto a selected one of said first and second storage structures;

a first insert logic coupled to said first and third storage structures to selectively merge said undiverted ones and said insertion ones of said ingress packets; and

a register interface, including packet packing and unpacking logic, coupled to the second and third storage structures to facilitate retrieval by a processor said diverted ones of said ingress packets in unpacked portions, and provision by said processor said insertion ones of said ingress packets in unpacked portions.

34. The buffering structure of claim 33, wherein said buffering structure further comprises

a fourth storage structure to stage undiverted ones of egress packets;

a fifth storage structure to stage diverted ones of egress packets;

a second divert logic coupled to said fourth and fifth storage structures to selective route egress packets onto a selected one of said fourth and fifth storage structures; and

said register interface, also coupled to the fifth storage structure to facilitate retrieval by said processor said diverted ones of said egress packets in unpacked portions.

35. The buffering structure of claim 33, wherein

said buffering structure further comprises

a fourth storage structure to stage undiverted ones of egress packets,

a fifth storage structure to stage insertion ones of egress packets, and

an insertion logic coupled to the fourth and fifth storage structures to selective merge said undiverted ones and said insertion ones of said egress packets; and

said register interface is further coupled to said firth storage structures to facilitate provision to said fifth storage structure by said processor said insertion ones of said egress packets in unpacked portions.

36. A buffering structure comprising:

a first storage structure to stage undiverted ones of ingress packets;

a second storage structure to stage diverted ones of ingress packets;

a third storage structure to stage undiverted ones of egress packets;

a fourth storage structure to stage diverted ones of egress packets;

a first divert logic coupled to said first and second storage structures to selectively route ingress packets onto a selected one of said first and second storage structures;

a second divert logic coupled to said third and fourth storage structures to selectively route egress packets onto a selected one of said third and fourth storage structures; and

a register interface, including packet unpacking logic, coupled to the second and fourth storage structures to facilitate retrieval by a processor said diverted ones of said ingress and egress packets in unpacked portions.

37. The buffering structure of claim 36, wherein

said buffering structure further comprises

a fifth storage structure to stage insertion ones of ingress packets,

an insertion logic coupled to the first and fifth storage structures to selective merge said undiverted ones and said insertion ones of said ingress packets; and

said register interface is further coupled to said firth storage structures to facilitate provision to said fifth storage structure by said processor said insertion ones of said ingress packets in unpacked portions.

38. The buffering structure of claim 36, wherein

said buffering structure further comprises

a fifth storage structure to stage insertion ones of egress packets, and

an insertion logic coupled to the third and fifth storage structures to selective merge said undiverted ones and said insertion ones of said egress packets; and

said register interface is further coupled to said firth storage structures to facilitate provision to said fifth storage structure by said processor said insertion ones of said egress packets in unpacked portions.

39. A buffering structure comprising:

a first storage structure to stage undiverted ones of ingress packets;

a second storage structure to stage insertion ones of ingress packets;

a third storage structure to stage undiverted ones of egress packets;

a fourth storage structure to stage insertion ones of egress packets;

a first insertion logic coupled to the first and second storage structures to selective merge said undiverted ones and said insertion ones of said ingress packets;

a second insertion logic coupled to the third and fourth storage structures to selective merge said undiverted ones and said insertion ones of said egress packets; and

a register interface, including packet packing logic, coupled to the second and fourth storage structures to facilitate provision by a processor said insertion ones of said ingress and egress packets in unpacked portions.

40. The buffering structure of claim 39, wherein

said buffering structure further comprises

a fifth storage structure to stage diverted ones of ingress packets,

a divert logic coupled to the first and fifth storage structures to selectively route ingress packets onto a selected one of said first and fifth storage structures; and

said register interface is further coupled to said firth storage structures to facilitate retrieval by said processor said diverted ones of said ingress packets in unpacked portions.

41. The buffering structure of claim 39, wherein

said buffering structure further comprises

a fifth storage structure to stage diverted ones of egress packets,

a divert logic coupled to the third and fifth storage structures to selectively route egress packets onto a selected one of said third and fifth storage structures; and

said register interface is further coupled to said firth storage structures to facilitate retrieval by said processor said diverted ones of said egress packets in unpacked portions.